REMARKS

Amendments to the Claims

Claims 1-47 are pending. Claim 17 was amended to correct a typographical error. Claims 1, 8-10, 38-42, 44 and 46 were amended to clarify that the precharge voltage is applied to the channel through the substrate/substrate tub.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-6, 15-16, 38-39 and 44-47 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sakui et al. (U.S. Patent No. 6,049,494). Applicant respectfully traverses this rejection and submits that claims 1-6, 15-16, 38-39 and 44-47 are allowable for at least the following reasons.

Applicant respectfully maintains that Sakui et al. discloses a NAND Flash memory that utilizes a boosted bitline programming method which precharges carriers in the channel of the NAND string selected to be programmed by applying a precharge voltage to the bitline coupled to the NAND string. Applicant has also carefully reviewed the reference and has not found reference to precharging carriers in the channel of a NAND string selected to be programmed through the intrinsic diodes of the sources/drains of the NAND string from a precharge voltage applied to the substrate tub in Sakui et al., as maintained by the Examiner. The Applicant thus submits that the boosted bitline programming method of the NAND architecture Flash memory of Sakui et al. does not correspond to Applicant's boosted tub programming method which precharges carriers in the channel of a NAND floating gate memory cell string by coupling the precharge voltage through the substrate or substrate tub. *See, e.g.*, Sakui et al., Figures 9 and 14; Column 17, lines 45-54; Abstract. Applicant therefore respectfully submits that Sakui et al. does not teach or disclose a NAND architecture Flash memory that precharges carriers in the floating gate transistors of one or more NAND memory cell strings by coupling a precharge voltage to the channels of the floating gate transistors through the substrate tub.

Applicant's claim 1 recites, in part, "coupling a precharge voltage through a substrate tub to a plurality of channels of a plurality of floating gate memory cells of a NAND architecture memory array, wherein the plurality of floating gate memory cells are coupled in a plurality of

strings." As detailed above, Applicant submits that Sakui et al. fails to teach or disclose such a method that generates carriers in the channels of one or more NAND memory cell strings by coupling the precharge voltage to the channels through the substrate tub. As such, Sakui et al. fails to teach or disclose all elements of independent claim 1.

Applicant's claim 38 recites, in part, "precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to the NAND architecture floating gate memory string through a substrate that is coupled to the NAND memory string." As detailed above, Applicant submits that Sakui et al. fails to teach or disclose such a method that generates carriers in the channels of one or more NAND memory cell strings by coupling the precharge voltage to the channels through the substrate tub. As such, Sakui et al. fails to teach or disclose all elements of independent claim 38.

Applicant's claim 44 recites, in part, "applying a precharge voltage through a substrate tub to a plurality of channels of a plurality of floating gate memory cells of the NAND architecture memory array, wherein the plurality of floating gate memory cells are serially coupled source to drain in a plurality of strings." As detailed above, Applicant submits that Sakui et al. fails to teach or disclose such a method that generates carriers in the channels of a NAND memory cell string by coupling the precharge voltage to the channels through the substrate tub. As such, Sakui et al. fails to teach or disclose all elements of independent claim 44.

Applicant's claim 46 recites, in part, "generating a channel of carriers in the floating gate transistor memory cell by coupling a precharge voltage to a channel region of the floating gate transistor memory cell through on a substrate tub the floating gate transistor memory cell is formed on." As detailed above, Applicant submits that Sakui et al. fails to teach or disclose such a method that generates carriers in the channel of one or more floating gate memory cells by coupling the precharge voltage to the channels through the substrate tub. As such, Sakui et al. fails to teach or disclose all elements of independent claim 46.

Applicant respectfully contends that claims 1, 38, 44 and 46 have been shown to be patentably distinct from the cited reference. As claims 2-6, 15-16, 39, 45 and 47 depend from and further define claims 1, 38, 44 and 46, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 1-6, 15-16, 38-39 and 44-47.

Allowable Subject Matter

Claims 17-37 were allowed.

Claims 7-14 and 40-43 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Claims 7-14 and 40-43 depend from the rejected base claims 1 and 38, respectively. As stated above, Applicant has amended claims 1 and 38 to clarify that the precharge voltage is applied to the channel through the substrate tub to overcome the cited reference Sakuui et al. As such, claims 1 and 38 are deemed to be in condition for allowance. As claims 7-14 and 40-43 depend from and further define claims 1 and 38, they are also considered to be in condition for allowance. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claims 7-14 and 40-43.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250